MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2015/2016

DCS5048 – COMPUTER SYSTEMS ARCHITECTURE

(DIT Students Only)

5 MARCH 2016
9.00 a.m. – 11.00 a.m.
(2 Hours)

INSTRUCTIONS TO STUDENT:

1. This booklet consists of **SIX (6)** pages excluding the cover page. There are **TWO (2)** sections in this booklet.

2. **SECTION A**: There are **TWENTY (20)** Multiple Choice Questions (MCQ) (20 marks). Answer **ALL** questions on the OMR sheet provided.

3. **SECTION B**: There are **THREE (3)** structured questions (60 marks). Answer **ALL** questions in the answer booklet provided.

SECTION A: MULTIPLE CHOICE QUESTIONS (MCQ) (20 Marks)

Instruction: *Answer **ALL** the questions in this section and shade your answers on the OMR sheet provided.*

1. The significant milestone of the third generation computer was the introduction of _____ in the production of the CPU.
   A. integrated circuit
   B. transistor
   C. registers
   D. cache

2. Which of the following statements are **TRUE** about computer organization?
   I. Instruction set, number of bits used to represent various data types, I/O mechanisms, techniques for addressing memory.
   II. Attributes of a system visible to the programmer.
   III. Hardware details transparent to the programmer, control signals, interfaces between the computer and peripherals, memory technology used.
   IV. The operational units and their interconnections that realize the architectural specifications.

   A. II and III
   B. II, III and IV
   C. III and IV
   D. All of the above

3. Which of the following is **FALSE** about the ENIAC?
   A. Programmed manually by switches
   B. Low power consumption
   C. Uses 18,000 vacuum tubes
   D. Uses decimal representation

4. Which of the following is **NOT** an example of interrupt?
   A. Arithmetic overflow
   B. Memory parity error
   C. Illegal timer
   D. Power failure

5. What is the value of 1155655_8 in hexadecimal representation?
   A. $4DBCD_{16}$
   B. $4DCBA_{16}$
   C. $4DBAD_{16}$
   D. $4DABC_{16}$

Continued.....

6. What is the value of 100111.11_2 in octal representation?
   A. 47.6_8
   B. 39.75_8
   C. 47.7_8
   D. 48.6_8

7. What is -20 in two's complement with 6-bit representation?
   A. 010100_2
   B. 101100_2
   C. 101011_2
   D. 010011_2

8. Which of the following is the normalized floating point format for 0.011001_2?
   A. 1.1001×2^3
   B. 1.1001×2^{-3}
   C. 1.1001×2^{-2}
   D. 1.1001×2^2

9. Which of the following is the postfix notation for [E – (J + M)] / (H * O)?
   A. E J M + – H O * /
   B. E J M H O – + / *
   C. J M E + – H O / *
   D. J M E – + / * H O

10. Which of the following addressing modes is similar to direct addressing but the address field refers to a register rather than a main memory address?
    A. Immediate addressing
    B. Indirect addressing
    C. Displacement addressing
    D. Register addressing

11. Which of the following are **TRUE** about random access method?
    I. Access must be made in a specific linear sequence
    II. Individual addresses identify locations exactly
    III. Data is located by a comparison with contents of a portion of the store
    IV. Access time is independent of location or previous access

    A. I and II
    B. I and IV
    C. II and III
    D. II and IV

Continued.....

12. Once the cache has been filled, when a new block is brought into the cache, one of the existing blocks must be replaced. Which of the following replacement algorithms replaces the block in the set that has experienced the fewest references?
    A. Least Recently Used (LRU)
    B. First-In-First-Out (FIFO)
    C. Least Frequently Used (LFU)
    D. Random

13. For random-access memory, _____ is the time it takes to perform a read or write operation.
    A. access time
    B. memory cycle time
    C. transfer rate
    D. average time

14. _____ is the highest-level bus that the chipset uses to send information to and from the processor.
    A. Memory bus
    B. System bus
    C. Cache bus
    D. Local I/O bus

15. Which of the following characteristics of bus refers to the total amount of data that can theoretically be transferred on the bus in a given unit of time?
    A. Bus width
    B. Bus speed
    C. Bus bandwidth
    D. Transfer time

16. Which of the following are categories of external devices?
    I. Human readable
    II. Machine readable
    III. Communication
    IV. Memory

    A. I, II and III
    B. I, II and IV
    C. I, III and IV
    D. II, III and IV

Continued.....

17. Which of the following are disadvantages of Programmed I/O technique?
    I. Time consuming
    II. Keeps the processor busy needlessly
    III. Unpredictable occurrence of interrupts
    IV. I/O module gains direct access to memory

    A. I and II
    B. I and III
    C. II and III
    D. II and IV

18. _____ uses a daisy chain configuration, with up to 63 devices connected to a single port.
    A. Universal Serial Bus
    B. FireWire Serial Bus
    C. InfiniBand
    D. Thunderbolt

19. A _____ occurs when two or more instructions that are already in the pipeline need the same resource.
    A. data hazard
    B. control hazard
    C. resource hazard
    D. instruction hazard

20. Which of the following are characteristics of Reduced Instruction Set Architecture?
    I. Simple instruction formats
    II. Simple addressing modes
    III. Register-to-register operations
    IV. One instruction per cycle

    A. I, II and III
    B. I, II and IV
    C. II, III and IV
    D. All of the above

SECTION B: STRUCTURED QUESTIONS (60 Marks)

Instruction: *Answer **ALL** the questions in this section and write your answers in the answer booklet provided.*

QUESTION 1 (20 Marks)

a) Given the memory contents and the opcodes as shown below, assume that currently Program Counter (PC) holds 701, execute the next **FOUR (4)** instructions and show the contents of all **THREE (3)** registers (Program Counter – PC, Instructions Register – IR and Accumulator – AC) and any changes made to the memory at the end of the instruction execution.

Address	Contents
701	1851
702	5930
703	2940
704	6950
851	0135
930	013A
940	
950	01AB

Original memory contents

Instruction	Meaning
0001	Load AC from memory
0010	Store AC to memory
0101	Add to AC from memory
0110	Subtract memory from AC

Partial list of opcodes

[10 Marks]

b) Perform the following conversions. All the necessary steps to obtain the answers must be shown.

i. Convert AC_{16} to its octal equivalent. [2 Marks]
ii. Convert 110101011.01101_2 to its hexadecimal equivalent. [2 Marks]

c) Calculate $-175_{10} + 100_{10}$ using ***two's complement*** with ***8-bit*** data representation. [6 Marks]

Continued.....

QUESTION 2 (20 Marks)

a) Given the following expression,

$$Y = [A * (N - F / I)] * [E / (L - D)]$$

i. Convert the expression to postfix notation. [1 Mark]
ii. Write the following machine instructions:
- Two-address [2.5 Marks]
- Three-address [2.5 Marks]

iii. Draw the stack diagrams that illustrate the program execution. [4 Marks]

b) A computer system has a memory architecture made up of main memory of 8GB and cache of 840KB. In order to perform an efficient mapping function, the main memory is arranged in blocks of 120 bytes.

Draw the address structures for different mapping functions as stated below. Indicate the fields and the number of bits required for each field.

i. Direct Mapping [3.5 Marks]
ii. Four-Way Set Associative Mapping [3.5 Marks]
iii. Associative Mapping [3 Marks]

QUESTION 3 (20 Marks)

a) What is Peripheral Component Interconnect Express (PCIe)? State **TWO (2)** key requirements for PCIe. [4 Marks]

b) List and explain any **THREE (3)** general categories of techniques used to handle multiple interrupts. [6 Marks]

c) Given **FIVE (5)** instructions where each instruction has **FOUR (4)** stages (FI, DI, EI, WO) with delays of 8, 4, 5, and 5 seconds for each stage respectively.

i. Draw a timing diagram for instruction pipeline operation. [5 Marks]

ii. Calculate the **total processing time**, **speedup** and **throughput** for the implementation of pipelining and non-pipelining. [5 Marks]
[Note: Please write the formula that is appropriate to use]

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